

**PRODUCT SPECIFICATION****TFT-LCD MODULE****Module No: 312261-01**☒ Preliminary Specification☐ Approval Specification

Designed by	Checked by	Approved by

Final Approval by Customer

Approved by	Comment

For more information, contact us:

WWW.DCLTEK.COM | 1-800-407-8917 | SALES@DCLTEK.COM

※The specification of "TBD" should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.

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1.Document Revision History

Version	Contents	Date	Note
V0	Original	2021.09.16	
V1	Update camera lens position	2022.03.25	
V2	Change the driver IC and cover material	2022.03.28	
V3	Update radius and size of the glass	2022.06.15	

1.0 General Description

1.1 Introduction

312261-01 color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel and a driving circuit. This TFT LCD has a 5.0 inch diagonally measured active display area with (720 horizontal by 1280 vertical pixel) resolution.

1.2. Features

5.0 inch configuration

Image Reversion: UP/DOWN and LEFT/RIGHT

ROHS design

1.3. General information

Item	Specification	Unit
LCM+CTP Outline Dimension	76.00(H) x 141.20(V) x3.35(D)	mm
Display area	62.10(H) x 110.40(V)	mm
Number of Pixel	720(H) x 1280 (V)	pixels
Pixel pitch	0.08625(H) x(RGB)x0.08625 (V)	mm
Pixel arrangement	RGB Vertical stripe	
Display mode	IPS(Normal Black)	
Color Filter Array	RGB vertical stripes	
Weight	TBD	g
Interface	MIPI	

2.0 Outline dimension

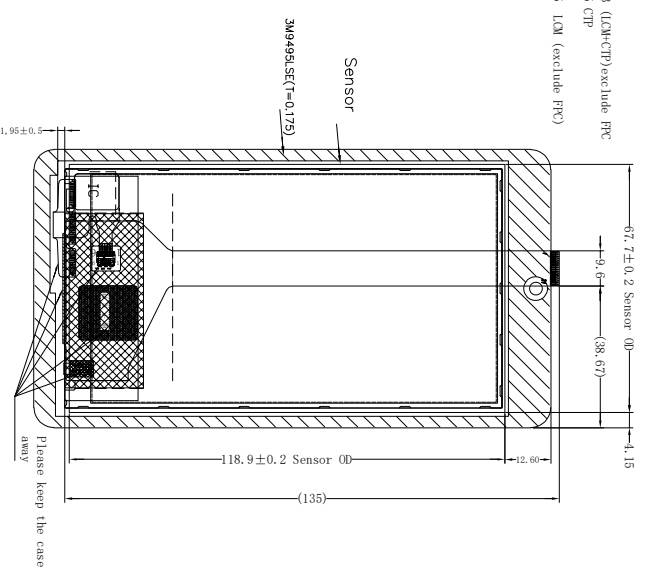
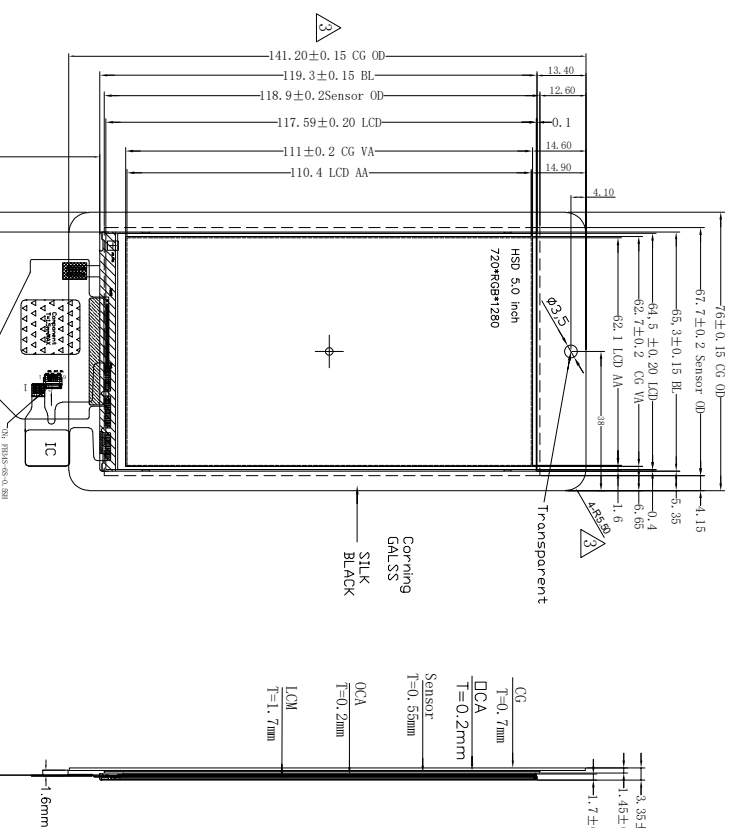
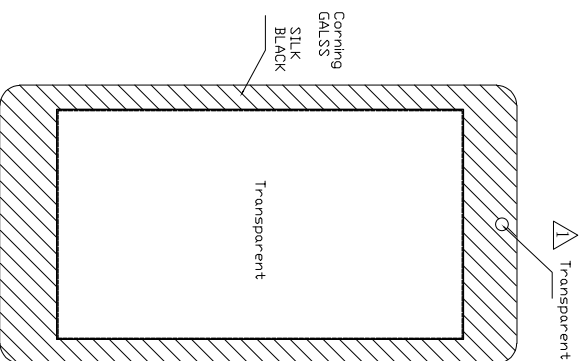
LCM+CTP

Front view

Side view

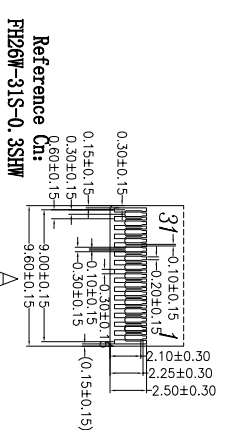
Back view

Display Pin interface



FPC bending diagram

FPC bending shipping



1	GND
2	TOUCH_3V3
3	GND
4	TOUCH_INT
5	TOUCH_RST
6	TOUCH_SDA
7	TOUCH_SCL
8	GND
9	LED-
10	LED+
11	ID
12	RSTN
13	NC
14	IOWCC_1.8
15	VCC_2.8
16	GND
17	D3P
18	D3N
19	GND
20	D2P
21	D2N
22	GND
23	CKP
24	CKN
25	GND
26	D1P
27	D1N
28	GND
29	D0P
30	D0N
31	GND

CTP NOTE:

1. LENS+OCA+ITO GLASS+FPC

ITO GLASS: 0.55mm

LENS GLASS: 0.7mm, Asahi; $\sqrt{2}$

IC: 6T911

2. Operation Voltage: CTP VCC 2.8V-3.3 V

4. The cover hardness: 6H

- *5. Please add mill-resistors on

the motherboard for SDA and SCL.

Notes:

1. Display : 5.0"HD, HSD TFT-IPS
2. Resolution: 720xRGBx1280
3. LCD Viewing Direction: ALL,
4. Display Mode: Normally Black/Transmissive
5. LCD Driver: HX8394F (without RAM) need to be adjusted by customer mainboard for landscape use. 

6. LCM+CTP brightness average: $260\text{cd/m}^2(\text{Typ})$, Uniformity $\geq 80\%$

7. Unmarked tolerance: ± 0.2

8 OPERATING TEMP.: -10°C to $+60^{\circ}\text{C}$

9. STORAGE TEMP.: -20°C to $+70^{\circ}\text{C}$

10. Requirements on Environmental Protection: ROHS

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3	Update radius and size of the glass	2022. 06. 14	
2	Change the driver IC and cover material	2022. 03. 28	
1	Update camera lens position	2022. 03. 25	
0	First issue	2021. 9. 16	
REV	DESCRIPTION	DATE	NAME

SCALE: 1/1	UNIT: mm	PAGE: 1/1		Approve	Check	Drawn
Part No:	312261-01		VER: V3			
Customer No.						

DCU

PIN	Name
1	VDD(3.3V)
2	GND
3	INT(3.3V)
4	RST(3.3V)
5	SDA(3.3V)
6	SCL 3.3V

TP-PIN

mipi interface

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3.0 Interface pin define

LCM Interface PIN Define:

Pin No.	Symbol	Description	Remark
1	GND	Power Ground	
2	TOUCH_3V3	Touch Panel Power supply	
3	GND	Power Ground	
4	TOUCH_INT	An interrupt signal to inform the host processor that touch data is ready for read	
5	TOUCH_RST	Touch Panel Reset Signal PIN	
6	TOUCH_SDA	Serial Data Input And Output	
7	TOUCH_SCL	Serial Clock Input	
8	GND	Power Ground	
9	LEDK	Power for LED backlight (Cathode)	
10	LEDA	Power for LED backlight (Anode)	
11	ID	ID PIN Pull High, If not use, please not connect	
12	RESET	Global reset signal(Follow IOVCC voltage)	
13	NC	No connect	
14	IOVCC_1V8	Digital power=1.8V	
15	VDD_3V3	Power supply=2.8-3.3V	
16	GND	Power Ground	
17	D3P	MIPI-D3Pare differential small amplitude signals	
18	D3N	MIPI-D3Nare differential small amplitude signals	
19	GND	Power Ground	
20	D2P	MIPI-D2Pare differential small amplitude signals	
21	D2N	MIPI-D2Nare differential small amplitude signals	
22	GND	Power Ground	
23	CLKP	MIPI-CLKPare differential small amplitude signals	
24	CLKN	MIPI-CLKNare differential small amplitude signals	
25	GND	Power Ground	
26	D1P	MIPI-D1Pare differential small amplitude signals	
27	D1N	MIPI-D1Nare differential small amplitude signals	
28	GND	Power Ground	

29	D0P	MIPI-D0Pare differential small amplitude signals	
30	D0N	MIPI-D0Nare differential small amplitude signals	
31	GND	Power Ground	

Touch Panel Interface PIN Define:

Pin No.	Symbol	Description	Remark
1	TOUCH_3V3	Touch Panel Power supply	
2	GND	Power Ground	
3	TOUCH_INT	An interrupt signal to inform the host processor that touch data is ready for read	
4	TOUCH_RST	Touch Panel Reset Signal PIN	
5	TOUCH_SDA	Serial Data Input And Output	
6	TOUCH_SCL	Serial Clock Input	

4. Operation Specifications

4.1 Absolute Maximum Ratings

Electrical Maximum Ratings (VSS=0V)

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage	VDD3V3	2.8	3.6	V	
	IOVCC	1.65	3.6	V	

Note: 1. VCI, GND must be maintained.

2. The modules may be destroyed if they are used beyond the absolute maximum ratings.

3. Ta=25+/-2.

4.2. 1 Electrical Specifications(Typical Operation Conditions, At Ta = 25 °C)

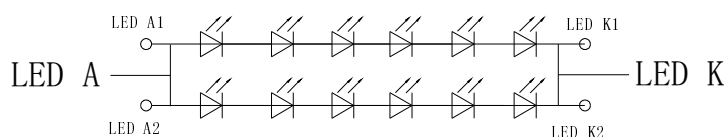
ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Power Supply Voltage	IOVCC	1.7	1.8	1.9	V	-
	VDD3V3	2.8	3.3	3.6	V	-

4.3.1 Back-light Unit:

PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
LED Current	IF	—	40	—	mA	—	—
Luminous	--	--	260		cd/m ²	I=40mA	
LED Voltage	VF	17.1	19.2	21	V	I=40mA	—
Life Time		—	20000	—	Hr.	I=40mA	
Color	White						

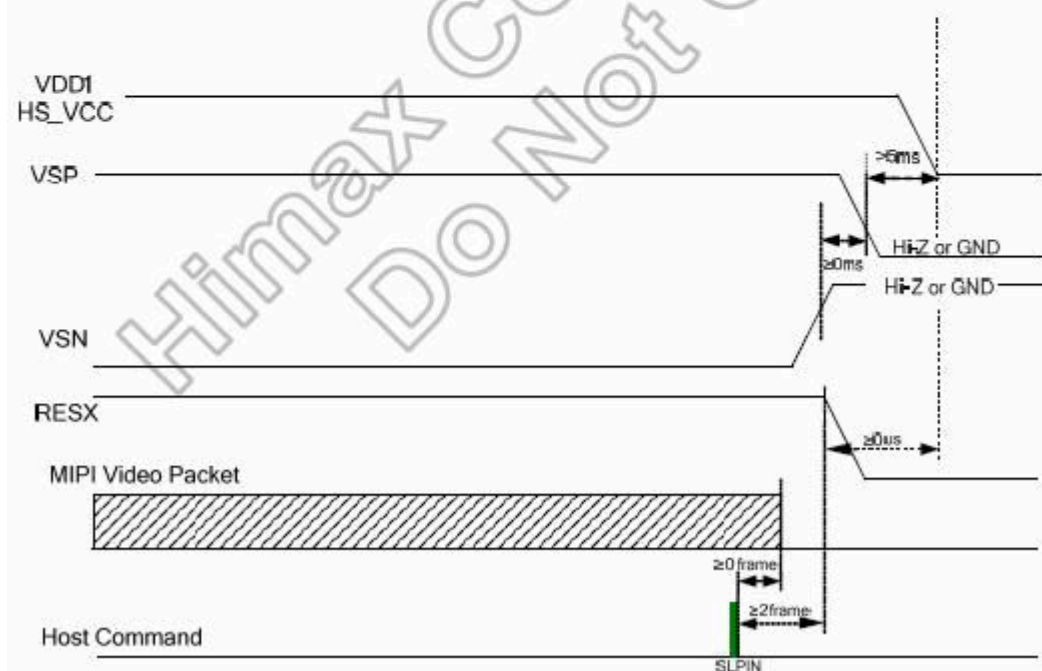
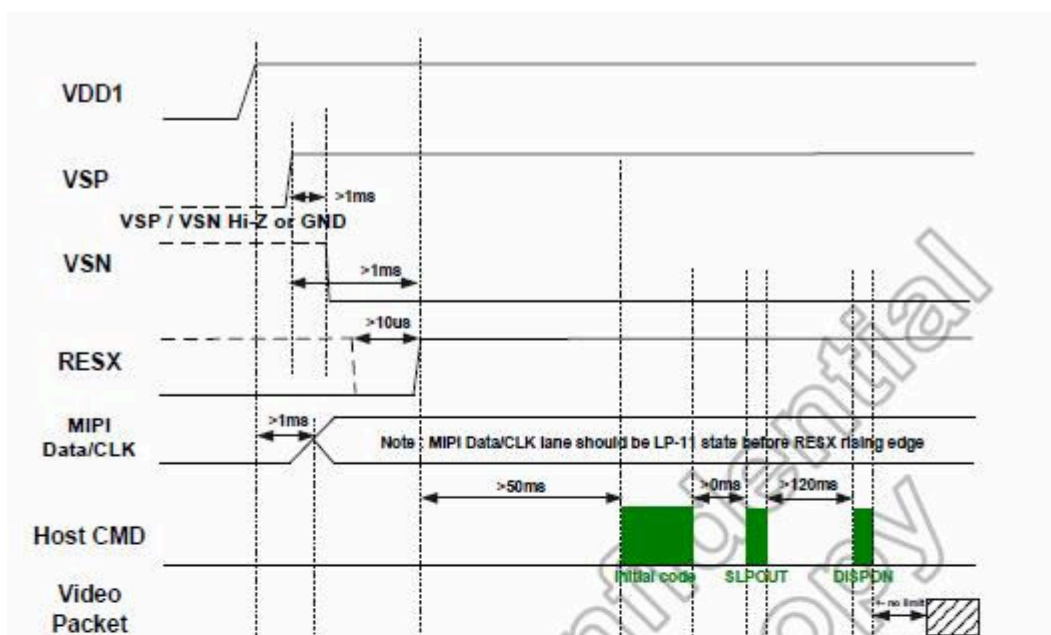
Note (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IF =40mA. The LED lifetime could be decreased if operating IF is larger than=40mA.



Circuit Diagram
IF=2*20mA=40mA

4.3.2 Power on/off Sequence



4.4 DSI system interface

The selection of interface is by BS[2:0]="000"~"111" the DSI specifies the interface between a host processor and a peripheral such as a display module. Figure 4.5 shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface also sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events.

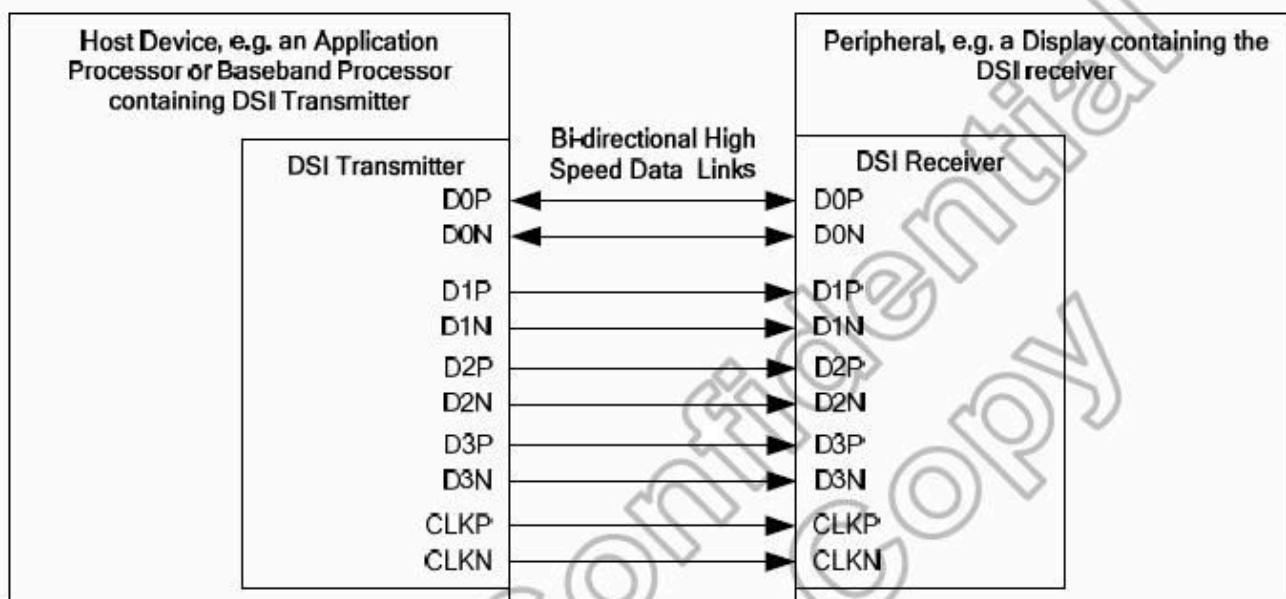


Figure 4.5: DSI transmitter and receiver interface

Please refer to "**DRAFT MIPI Alliance Standard for DSI**" for DSI detail specifications.

The data lane number is selected by register RBAh.

4.4.1 DSI layer definitions

According Figure 4.6 DSI transmitter and receiver interface to understand simple interface block diagram. Then under diagram is internal block for DSI which include four layers: PHY Layer, Lane Management Layer, Low level protocol and Application Layer.

The PHY Layer specifies the characteristics of transmission medium and electrical parameters for signaling the timing relationship between clock and Data Lanes.

The Lane Management Layer specifies DSI is Lane-scalable for increased performance. The data signals maybe transmission through one or more channel depending on the bandwidth requirements of the application.

The Protocol Layer specifies at the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets.

The Application Layer describes higher-level encoding and interpretation of data contained in the data stream. The DSI specification describes the mapping of pixel values, commands and command's parameters to bytes in the packet assembly.

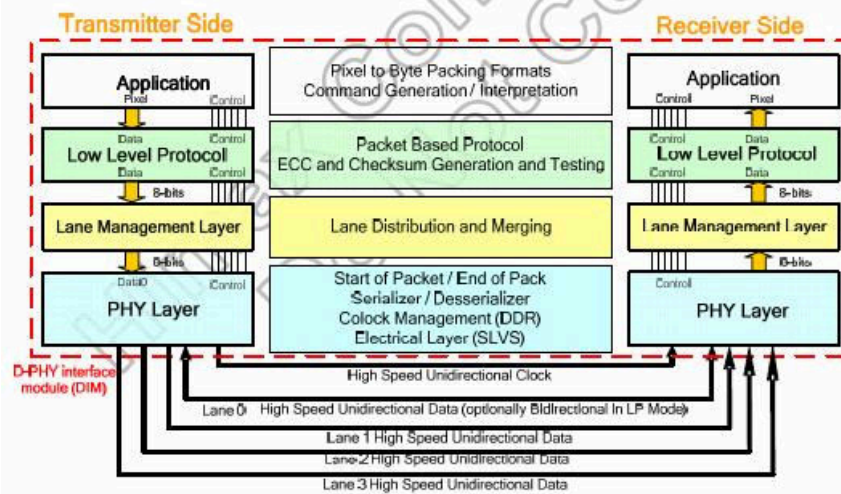


Figure 4.6: DSI transmitter and receiver interface

4.4.2 Lane states

The HX8394-F uses Data Lane and Clock Lane differential pairs for DSI. Both differential lane pairs can be driven LP (Low Power) or HS (High Speed) mode.

LP mode means each line of the differential pairs are used in independently and single-ended. In LP mode differential receiver is disable (Termination resistor of the receiver is disable). In LP mode there are four possible Low-Power Lane states (LP-00, LP-01, LP-10, LP-11).

HS mode means the differential pairs are not used in single-end and termination resistor of the receiver is enable. There are different modes and protocol in each mode when transfer display data from MCU to the display module.

The state code of HS and LP Lane pair are defined as below:

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	Note1	Note1
HS-1	HS High	HS Low	Differential-1	Note1	Note1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	Note2

Note: (1) During High-Speed transmission the Low-Power Receivers observe LP-00 on the Lines.
(2) If LP-11 occurs during Escape mode the Lane returns to Stop state (Control Mode LP-11)

4.4.3 Clock lane mode

Figure 4.7 shows the state diagram for Clock Lane Mode. The Clock Lane has three different power modes: Low Power Stop State, Ultra Low Power State (ULPS) and High Speed clock transmission.

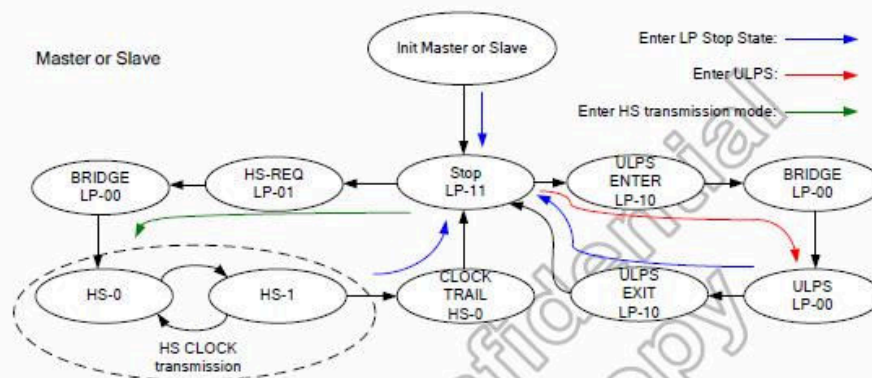
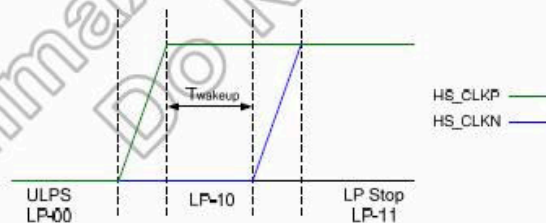


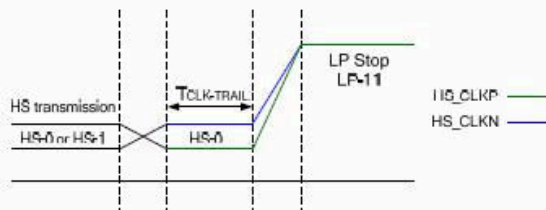
Figure 4.7: Clock lane mode state diagram

Clock Lane can be driven LP-11 to enter Low Power Stop State. There are three ways to enter Lower Power Stop State:

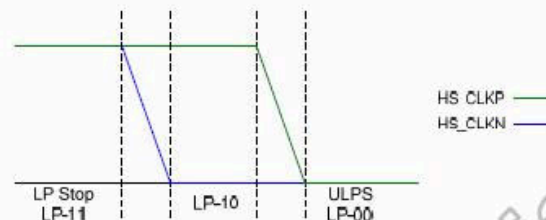
- (1) After Initial state. (HW reset, SW reset, Power on sequence)
- (2) Leaving ULPS: ULPS LP-00 → LP-10 → Low Power Stop State LP-11.



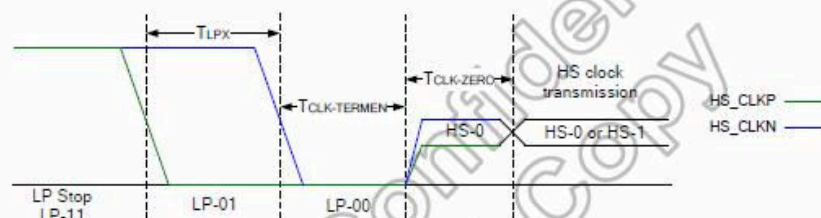
- (3) Leaving HS clock transmission mode: HS mode (HS-0 or HS-1) → HS-0 → Low Power Stop State LP-11.



Clock Lane can be driven LP-00 to enter Ultra Low Power State from Low Power Stop State. The flow is Low Power Stop State LP-11 → LP-10 → ULPS LP-00.



Clock Lane can be High Speed Clock transmission State from Low Power Stop State. The flow is Low Power Stop State LP-11 → LP-01 → LP-00 → HS-0/1.



4.4.4 Data lane mode

Figure 4.8 shows the operational flow diagram for Data Lane Mode. There are three operating modes in Data Lane: Escape mode, High-Speed transmission mode and Turnaround.

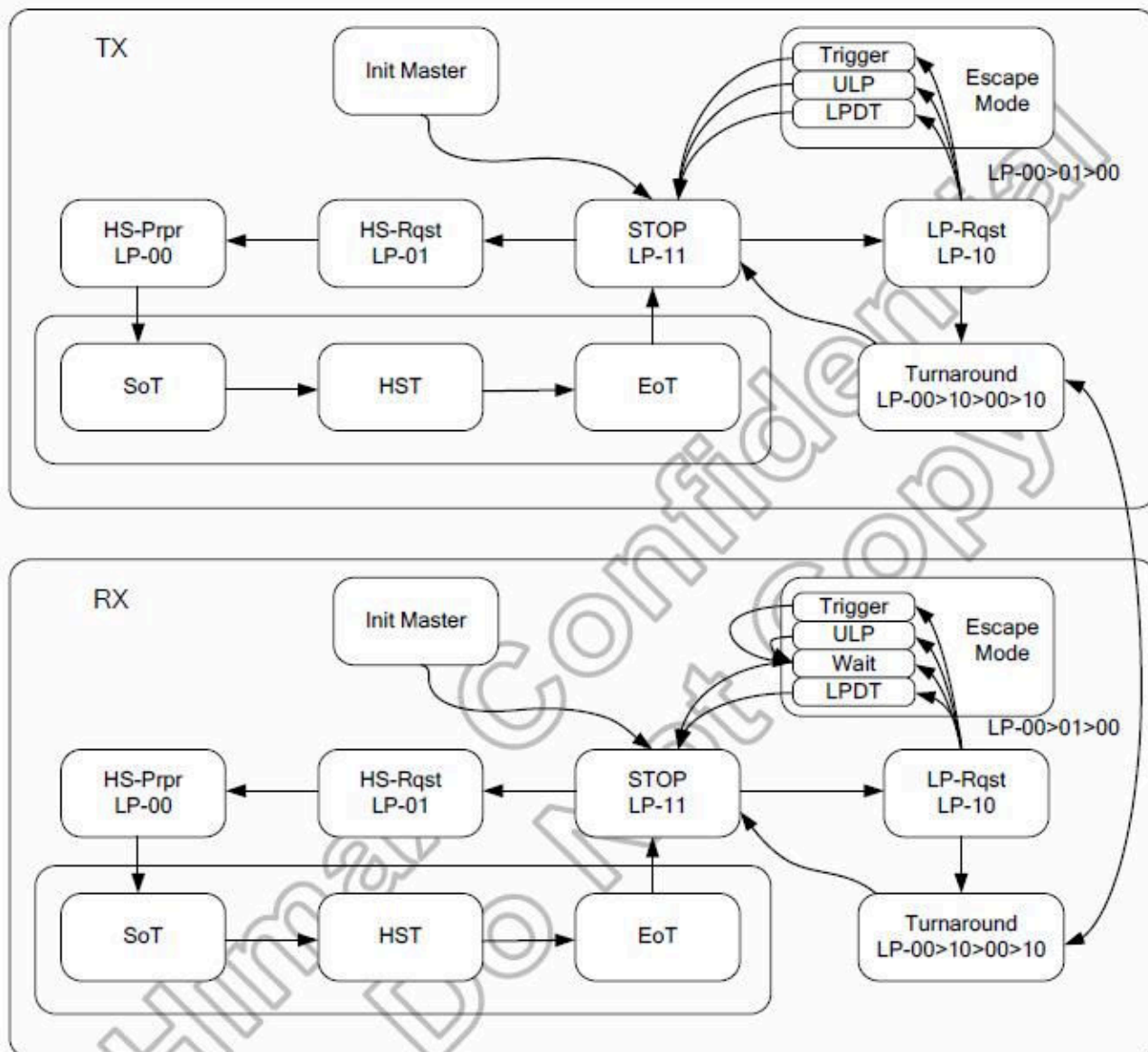
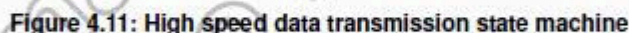


Figure 4.8: Data lane mode state diagram

The display module can enter High Speed Data Transmission when Clock Lane in the High Speed Clock Mode. All Data Lane enter High Speed Data Transmission synchronously but may end at different time. Data Lane enter High Speed Data Transmission flow: LP-11 -> LP-01 -> LP-00 -> SoT (0001_1101). And exit High Speed Data Transmission flow: Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS-TRAIL}$.



Parameter	Description	Min.	Typ.	Max.	Unit
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	$40+4*UI$		$85+6*UI$	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145+10*UI$			ns
T_{EOT}	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.			$105ns+12*UI$	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	$60ns+4*UI$			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns

Table 4.2: Global Operation Timing Parameters for Data Lane

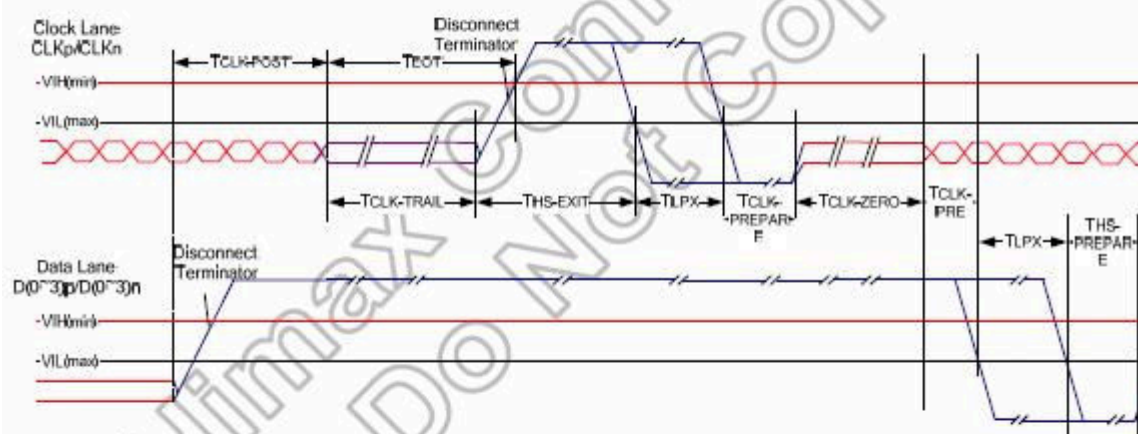


Figure 4.13: Switching the Clock Lane between Clock Transmission and LP Mode

Parameter	Description	Min.	Typ.	Max.	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	$60+52*UI$			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	60			ns
$T_{CLK-PREPARE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	38		95	ns

$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	$8*UI$			ns

Table 4.3: Global Operation Timing Parameters for Clock Lane

4.5 Timing for DSI video mode

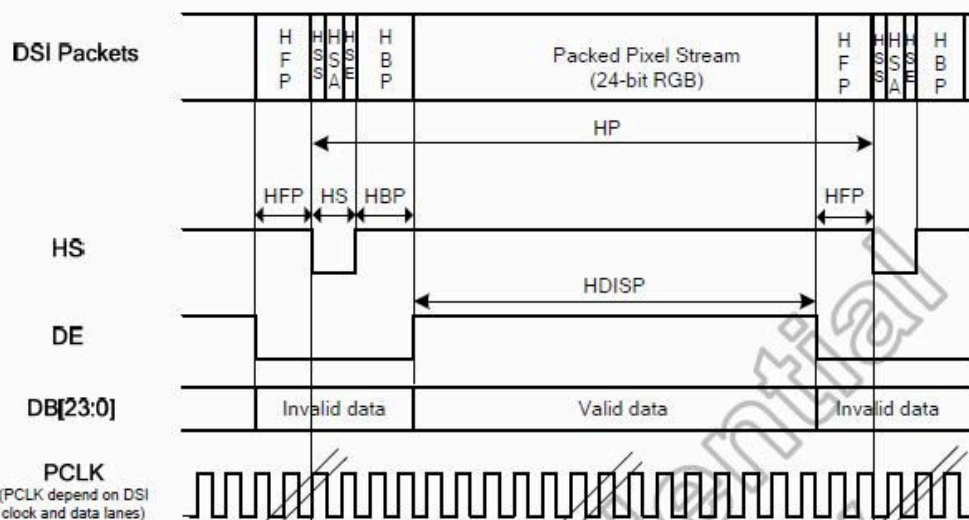


Figure 7.10: Horizontal timing for DSI video mode I/F

Resolution=720x1280 (VSSA=0V, VDD1=1.8V, VDD2=VDD3=VCC=2.8V, $T_A=25^\circ\text{C}$)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Horizontal cycle	HP	-	762	-	-	DCK
HS low pulse width	HS	-	6	-	-	DCK
Horizontal back porch	HBP	-	24	-	-	DCK
Horizontal front porch	HFP	-	12	-	-	DCK
Horizontal data start point	-	HS+HBP	30	-	-	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	12	-	-	DCK
Horizontal active area	HDISP	-	-	720	-	DCK

Note: (1) HS > 0.2 μs (12-DCK @ 352.8Mbps /4-lane, Frame rate 60Hz, min DSI CLK rate)
(18-DCK @ 540Mbps /4-lane, Frame rate 60Hz, max DSI CLK rate)
(2) HBP > 0.4 μs (24-DCK @ 352.8Mbps /4-lane, Frame rate 60Hz, min DSI CLK rate)
(36-DCK @ 540Mbps /4-lane, Frame rate 60Hz, max DSI CLK rate)
(3) HFP > 0.2 μs (12-DCK @ 352.8Mbps /4-lane, Frame rate 60Hz, min DSI CLK rate)
(18-DCK @ 540Mbps /4-lane, Frame rate 60Hz, max DSI CLK rate)

Table 7.14: Horizontal timings for DSI video mode I/F

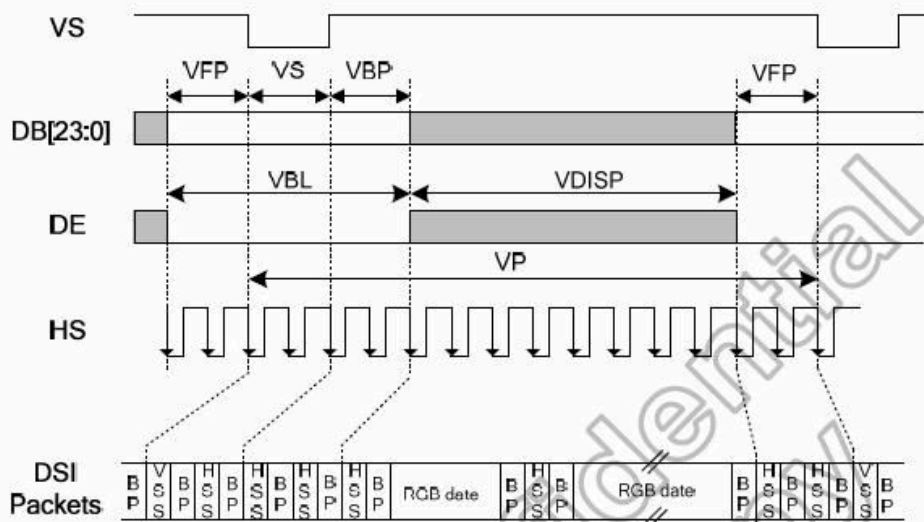


Figure 7.9: Vertical timings for DSI I/F

Resolution=720x1280(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25 °C)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Vertical cycle	VP	-	1286	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical data start point	-	VS+VBP	4	-	Note(1)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS/VBP/VFP pulse width are related to RD3h (Set GIP Option0). Please refer to the application note for VS/VBP/VFP setting.

Table 7.13: Vertical timings for DSI I/F

5.0 Optical specification

Table 6: Optical specifications

Items		Symbol	Condition	Specifications			Unit
				Min.	Typ.	Max.	
Contrast Ratio		CR		600	1000	-	-
Response Time		T _R +T _F		-	25	35	ms
Chromaticity	Red	X _R		-	-	-	-
		Y _R		-	-	-	-
	Green	X _G		-	-	-	-
		Y _G		-	-	-	-
	Blue	X _B		-	-	-	-
		Y _B		-	-	-	-
	White	X _W		0.268	0.290	0.328	-
		Y _W		0.269	0.300	0.329	-
Viewing angle	Hor.	Φ1(3 o'clock)	Center CR≥10	-	80	---	deg.
		Φ2(9 o'clock)		-	80	-	
	Ver.	θ2(12 o'clock)		-	80	-	
		θ1(6 o'clock)		-	80	-	
NTSC ratio				-	70		%

Note

Note

6.0 Reliability test items

NO	Item	Conditions	Remark
1	High Temperature Storage	Ta=+70℃,48hrs	
2	Low Temperature Storage	Ta=-20℃,48hrs	
3	High Temperature Operation	Ta=+60℃,48hrs	
4	Low Temperature Operation	Ta=-10℃,48hrs	
5	High Temperature and High Humidity (operation)	Ta=+40℃,90%RH,48hrs	

Note: All tests above are practiced at module type.

There is no display function NG issue occurred, All the cosmetic specification is judged before the reliability stress.

7.0 General Precaution

7.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

7.2 Assembly Precaytton

7.2.1 Please use the mounting hole on the module side in installing and do not bending or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.

7.2.2 Please design display housing in accordance with the following guide lines.

7.2.2.1 Housing case must be destined carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.

7.2.2.2 Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. The clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.

7.2.3 Please do not push or scratch LCD panel surface with any-thing hard. And do not soil LCD panel surface by touching with bare hands. (Polarizer film, surface of LCD panel is easy to be flawed.)

7.2.4 Please do not press any parts on the rear side such as source IC, gate IC, and FPC during handling LCD module. If pressing rear part is unavoidable, handle the LCD module with care not to damage them.

7.2.5 Please wipe out LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.

7.2.6 Please wipe out drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.

7.2.7 Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.

7.3 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. HannStar does not warrant the module, if customers disassemble or modify the module.

7.4 Breakage of LCD Panel

7.4.1 If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

7.4.2 If liquid crystal contacts mouth or eyes, rinse out with water immediately.

7.4.3 If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

7.4.4 Handle carefully with chips of glass that may cause injury, when the glass is broken.

7.5 Absolute Maximum Ratings and Power Protection Circuit

7.5.1 Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

7.5.2 Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

7.5.3 It's recommended employing protection circuit for power supply.

7.6 Operation

7.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead. Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

7.6.2 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

7.6.3 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

7.6.4 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

7.7 Static Electricity

7.7.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

7.7.2 Because LCD module uses CMOS-IC on TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge.

7.7.3 Persons who handle the module should be grounded through adequate methods.

7.8 Disposal

When disposing LCD module, obey the local environmental regulations.

7.9 OTHERS

7.9.1 A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior.

Please do not expose LCD module direct sunlight land strong UV rays.

7.9.2 Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.

7.9.3 For the packaging box, please pay attention to the followings:

7.9.3.1 Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.

7.9.3.2 Please do not pile them up more than 6 boxes. (They are not designed so.) And please do not turn over.

7.9.3.3 Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.

7.9.3.4 Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)